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MANUFACTURE OF ELEMENT ISOLATION REGION OF SEMICONDUCTOR**Publication Number:** 05-283404 (JP 5283404 A) , October 29, 1993**Inventors:**

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Applicants

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Application Number: 04-077062 (JP 9277062) , March 31, 1992**International Class (IPC Edition 5):**

- H01L-021/316
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JAPIO Class:

- 42.2 (ELECTRONICS--- Solid State Components)

JAPIO Keywords:

- R004 (PLASMA)
- R100 (ELECTRONIC MATERIALS--- Ion Implantation)

Abstract:

PURPOSE: To prevent a channel stopper layer under an element isolation film of a semiconductor device from diffusing into an element forming region, and form a mask for ion implantation to form the channel stopper layer in a self alignment manner.

CONSTITUTION: When the element isolation region of a semiconductor device is formed, a low stress silicon nitride film 4 is thickly deposited by a plasma CVD method, on a silicon nitride film 3 deposited by an LPCVD method, and an element isolation film 5 is formed by patterning and thermally oxidizing the silicon nitride film. Then channel stopper ions are implanted through the element isolation film 5 by using the thick silicon nitride film as a mask. (From: *Patent Abstracts of Japan*, Section: E, Section No. 1501, Vol. 18, No. 66, Pg. 15, February 03, 1994)

JAPIO

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Element isolation region forming in semiconductor device production - by implanting channel stopping ion using thick silicon nitride film as mask after high temperature heat treatment

NoAbstract

Patent Assignee: OKI ELECTRIC IND CO LTD

Patent Family

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Patent Details

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